REMARKS

This amendment is in response to the Examiner's Communication dated August 30, 2000.

Claims 1 through 39 are currently pending in the application, standing rejected.

With amendment of claims as provided herein above, and further in view of the arguments made hereinafter, the Applicant contends that claims 1 through 39 are in condition for allowance and the same is respectfully requested.

Claims 1, 7, 12 through 14, 20, 25 through 27, 33, 38 and 39 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshigai (U.S. Patent 5,606,199).

Claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32 and 34 through 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshigai as applied to claims 1, 7, 12 through 14, 20, 25 through 27, 33, 38 and 39, supra, and further in combination with Applicant's admitted prior art.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicant has amended claims 1 through 39 to clearly distinguish over the cited prior art.

35 U.S.C. § 102(b) Anticipation Rejections

Claims 1, 7, 12 through 14, 20, 25 through 27, 33, 38, and 39 were rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent 5,606,199, issued to Yoshigai (hereinafter "the Yoshigai reference").

Applicant submits that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicant submits that the Yoshigai reference does not expressly or inherently set forth each and every element in the presently claimed invention in the same detail that is contained in the presently amended claims.

The current application contains independent claims 1, 14 and 27 which all include the limitation that the paddle in the invention is attached to a side rail "by at least a plurality of paddle support bars and is further attached to a plurality of cross members by said support bars." This allows for precise positioning of the semiconductor device and makes it easier to insert and remove the semiconductor device.

The Yoshigai reference teaches an island 7, with a central recess 7a as a chip support section in which the semiconductor chip 4 is mounted. The Yoshigai reference fails to include the frame which includes the side rails, cross members and paddle which is attached to the side rails by paddle support bars and to cross members by paddle support bars that is described in the present set of independent claims. Thus, the Yoshigai reference fails to teach the enhancement of the ease of device handling that is taught in the present invention. Applicant respectfully disagrees with the Examiner's assessment that the Yoshigai reference teaches a paddle being attached to the side rail by a plurality of paddle support bars 3d and being attached to a plurality of cross members 3G by the support bars. Applicant asserts that 3d and 3g, shown in the Yoshigai reference, are ground and branch electrical leads that connect the electrode pads of a semiconductor chip to the lead frame. 3d and 3G are not structural members but serve to electrically connect the lead frame to a semiconductor. Further, the Yoshigai reference does not disclose a paddle. It discloses a central recess 7a as a chip support.

Additionally, the Yoshigai reference fails to show at least one conductive projection bump or a plurality of projection bumps 34 such as solder bumps or balls are formed on the bond pads 32, either expressly or inherently. Therefore, the Yoshigai reference fails to anticipate the present invention because it fails to teach every aspect of the independent claims of the present invention.

Because the Yoshigai reference fails to anticipate the presently claimed invention of novel independent claims 1, 14, and 27, dependent claims 7, 20,and 38 are not anticipated. Further, claims 12, 25, 33, and 39 are not anticipated by the Yoshigai reference because it fails to teach an assembly including a substrate containing at least one circuit on its upper surface.

Claims 13 and 26 are not anticipated since the claims they depend on are not anticipated. Therefore, Applicant requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b).

35 U.S.C. § 103(a) Obviousness Rejections

Claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yoshigai reference in view of the Applicant's admitted prior art.

Applicant submits that the combination of these references does not teach or suggest the presently claimed invention.

The Office Action states that although the Yoshigai patent does not explicitly teach the product of claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37, but that the Applicant's own application allegedly teaches that the product would be well known. Furthermore, the Office Action purports that it would have been obvious to combine the known products with the product of Yoshigai because it would facilitate connection of the die to the circuit substrate and the paddle.

The Applicant submits that the instant invention is not taught or suggested in the prior art. Applicant submits that a reference should be considered as a whole, and portions arguing against or teaching away from the claimed invention must be considered. Bausch & Lomb, Inc. v. BarnesHind/Hydrocurve, Inc., 230 USPQ 416 (Fed. Cir. 1986). The prior art references cited by the Examiner "would likely *discourage* the art worker from attempting the substitution suggested by [the applicant]." Gillette Co. v. S.C. Johnson & Son, Inc., 16 USPQ2d 1923 (Fed. Cir. 1990). The fact that the applicant achieved the claimed invention by doing what those skilled in the art had suggested should not be done is a fact strongly probative of nonobviousness. Kloster Speedsteel AB v. Crucible Inc., 230 USPQ 81 (Fed. Cir. 1986), on rehearing, 231 USPQ 160 (Fed. Cir. 1986). Additionally, "it is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teaching of the prior art so that the claimed invention is

rendered obvious . . . . One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fritch, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992).

Furthermore, Applicant submits that a *prima facie* case of obviousness has not established under 35 U.S.C. § 103. To establish a *prima facie* case of obviousness under 35 U.S.C. §103, the following criteria must be met:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

No Motivation or Suggestion to Combine Yoshigai with Admitted Prior Art

The Applicant respectfully disagrees with the Office Action's assessment of the Yoshigai reference. The Yoshigai reference fails to show conductive projections 34 such as solder bumps or balls are formed on the bond pads 32. In the present invention these projections enabling "gang" bonding, i.e. flip-chip bonding, of the semiconductor die bond pads to the conductive traces 46 of a substrate 42 such as a circuit board. Furthermore, the claims teach a semiconductor device assembly, comprising a semiconductor die having an active surface having a plurality of bond pads and an opposing second surface with at least one projection connected to at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die wherein the projection includes at least one solder ball and at least one solder bump. The invention also teaches a generally centrally positioned paddle of a lead frame of a plurality of lead frames having side rails and cross members connected to said paddle, wherein the generally centrally positioned paddle which is attached to the side rail by at a paddle support bar and is further attached to a cross members by the support bar. This is also not taught or suggested by

the Yoshigai reference nor the Applicant's admitted prior art. Thus, there is no motivation to combine the Yoshigai reference with any of the Applicant's admitted prior art.

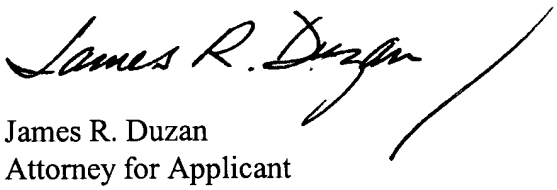
Therefore, the cited prior art, whether taken separately or whether combined as proposed in the proposed rejection, fails to establish a *prima facie* case of obviousness for the present invention as proposed to be claimed in claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37. Accordingly, claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37 are allowable.

Second, Applicant submits that at the very least, the proposed combination of the Yoshigai reference and the Applicant's admitted prior art does not teach or suggest all the limitations of the presently claimed invention to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. For instance, neither the Yoshigai reference nor Applicant's admitted prior art teaches or suggests such claim limitations calling for "at least one projection bump connected to at least a portion of the upper surface of at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die for direct connection to a substrate, said at least one projection bump including one of at least one solder ball and at least one solder bump", "wherein said at least one projection bump includes a plurality of projections comprising a ball grid array (BGA) of solder balls", "wherein said at least one projection bump comprises at least one ball deposited by a wire bonding machine", "wherein said at least one projection bump comprises at least one stud bump deposited by a wire bonding machine", "at least one projection bump secured to at least a portion of the upper surface said at least one bond pad on said active surface of said semiconductor die for direct connection to a substrate, said at least one projection bump including one of at least one solder ball and at least one solder bump", and "a plurality of [projections] projection bumps connected to at least a portion of the upper surfaces of said plurality of bond pads for direct connection to a host circuit board, said plurality of projections including one of a plurality of solder balls and a plurality of solder bumps".

Therefore, the proposed combination of the Yoshigai et al. reference and the Applicant's admitted prior art cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 with respect to the presently claimed invention of claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37. Accordingly, claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37 are allowable.

In summary, Applicant respectfully requests the allowance of claims 1 through 39 and the case passed for issue. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



James R. Duzan
Attorney for Applicant
Registration No. 28,393
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110
(801) 532-1922

Date: September 20, 2001

JRD/sls:djp

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Three Times Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon and an opposing second surface, each bond pad of said plurality of bond pads having an upper surface;

at least one projection bump connected to at least a portion of the upper surface of at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die for direct connection to a substrate, said at least one projection bump including one of at least one solder ball and at least one solder bump; and

to a host circuit board, each projection bump of said plurality of projection bumps located on at least a portion of the upper surface of a bond pad of said plurality of bond pads, each projection bump of said plurality of [projections] projection bumps including one of a [plurality] of solder ball [balls] and a [plurality] of solder bump [bumps]; and

a metallic paddle secured to said second surface of said semiconductor die, said metallic paddle being attached to at least one side rail by at least a plurality of paddle support bars and being attached to a plurality of cross members by said support bars a generally centrally positioned paddle of a lead frame of a plurality of lead frames having side rails and cross members connected to said paddle, said second surface of said semiconductor die being secured to said paddle; and said generally centrally positioned paddle being attached to the side rail by at least a plurality of paddle support bars and being attached to said cross members by said support bars.

2. (Amended) The semiconductor device assembly of claim 1, wherein said at least one projection bump includes a plurality of projections comprising a ball grid array (BGA) of solder balls.

3. (Amended) The semiconductor device assembly of claim 1, wherein said at least one projection bump comprises at least one ball deposited by a wire bonding machine.

4. (Amended) The semiconductor device assembly of claim 1, wherein said at least one projection bump comprises at least one stud bump deposited by a wire bonding machine.

14. (Three Times Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having at least one bond pad thereon and an opposing second surface, said at least one bond pad having an upper surface;

at least one projection bump secured to at least a portion of the upper surface said at least one bond pad on said active surface of said semiconductor die for direct connection to a substrate, said at least one projection bump including one of at least one solder ball and at least one solder bump; and

a metal paddle from a lead frame, said second surface of said semiconductor die being attached to said metal paddle; and said metal paddle is attached to at least one side rail by at least a plurality of paddle support bars and being attached to a plurality of cross members by said support bars.

15. (Amended) The semiconductor device assembly of claim 14, wherein said at least one projection bump comprises a ball grid array (BGA) of solder balls.

16. (Amended) The semiconductor device assembly of claim 14, wherein said at least one projection bump comprises at least one ball deposited by a wire bonding machine.

17. (Amended) The semiconductor device assembly of claim 14, wherein said at least one projection bump comprises at least one stud bump deposited by a wire bonding machine.

27. (Three Times Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon and an opposing second surface, each bond pad of said plurality of bond pads having an upper surface;

a plurality of [projections] projection bumps connected to at least a portion of the upper surfaces of said plurality of bond pads for direct connection to a host circuit board, said plurality of projections including one of a plurality of solder balls and a plurality of solder bumps; and

a metallic paddle secured to said second surface of said semiconductor die, said metallic paddle bing attached to at least one side rail by at least a plurality of paddle support bars and being attached to a plurality of cross members by said support bars.

28. (Amended) The semiconductor device assembly of claim 27, wherein each projection bump of said plurality of [projections] projection bumps comprises a ball grid array (BGA) of solder balls.

29. (Amended) The semiconductor device assembly of claim 27, wherein each projection bump of said plurality of [projections] bumps comprises balls deposited by a wire bonding machine.

30. (Amended) The semiconductor device assembly of claim 27, wherein each projection bump of said plurality of [projections] projection bumps comprises a plurality of stud bumps deposited by a wire bonding machine.